METHOD OF SELECTING PATTERN TO BE MEASURED, PATTERN INSPECTION METHOD, MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE, PROGRAM, AND PATTERN INSPECTION APPARATUS

Cross Reference to Related Application

This application claims benefit of priority under 35USC §119 to Japanese Patent Application No. 2002-362298, filed on December 13, 2002, the contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of selecting a pattern to be measured, a pattern inspection method, a manufacturing method of a semiconductor device, a program, and a pattern inspection apparatus, for example, to selection and inspection of a fine pattern to be measured in a manufacturing process of a semiconductor device.

Related Background Art

In a manufacturing process of a semiconductor device a scanning electron microscope apparatus, for example, a type called a critical dimension scanning electron microscope (CD-SEM) is used to inspect a dimension of a fine pattern. Moreover, an alignment deviation error of a pattern between layers is measured by an alignment deviation inspection apparatus.

Conventionally, a method of selecting a pattern to be measured depends heavily on a sequence of preparation of measurement schedule of a measurement device. In the method, several wafers to be measured are first selected from one lot, a semiconductor chip to be measured is then selected with respect to these wafers, and a measurement portion in the selected chip is defined. Thereafter, a dimension or alignment deviation is measured in the same measurement portion with respect to all the wafers to be measured and all the chips to be measured. As a result, the number of

wafers or chips constituting the measurement objects, and the total number of measurement portions in the chip are obtained by integration of these numbers. Therefore, when the wafer number, chip number, and in-chip measurement portions are simultaneously increased, a measurement cost exponentially increases.

As taught by a design of experiment method, this sampling strategy corresponds to a sampling strategy in which all alternate functions among factors such as fluctuations between the wafers and between the chips, and fluctuations in the chip are handled.

However, in actual, it is difficult to handle high-order alternate functions between the factors. Conversely, there has never been provided a factorial design method of performing measurement in which only the alternate functions to be handled are focused. Accordingly, there has never been provided a method of analyzing the fluctuations for each factor from measurement results obtained by the arrangement. Furthermore, in performing such a factorial design, it would have been remarkably difficult to prepare a measurement recipe in the above-described conventional measurement schedule preparation method.

BRIEF SUMMARY OF THE INVENTION

According to a first aspect of the present invention, there is provided a method of selecting a pattern to be measured comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer

numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point; and

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned.

According to a second aspect of the present invention, there is provided a pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and

selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

According to a third aspect of the present invention, there is provided a pattern inspection method using a measurement device, said method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured

based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned; and

actually measuring a standard pattern prepared beforehand a predetermined times using the measurement equipment, prior to an actual measurement to the defined measurement point to evaluate reliability of the measurement device.

According to a fourth aspect of the present invention, there is provided a manufacturing method of a semiconductor device using a pattern inspection method, said pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four

lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

According to a fifth aspect of the present invention, there is provided a program which allows a computer to implement a method of selecting a pattern to be measured, said selection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to

which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point; and

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned.

According to a sixth aspect of the present invention, there is provided a program which allows a computer to implement a pattern inspection method, said pattern inspection method comprising:

assigning first wafer numbers in order of a process to a wafer group constituted of a plurality of wafers including a semiconductor chip group respectively, the semiconductor chip group having a plurality of chips, each semiconductor chip having a pattern formed thereon in the process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two wafers having serial first wafer numbers from the first sub-groups to assign second wafer

numbers to the selected wafers, respectively;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-groups, further selecting a chip including the center position of the wafer inside thereof if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions the number of which exceeds the number of regions of at least two rows and two columns, on the basis of in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points from the pattern formed on the wafer as only one candidate measurement point with respect to the lattice points, and assigning a candidate measurement point number to the candidate measurement point;

defining only some of the candidate measurement points to which the candidate measurement point numbers have been assigned as first measurement points to be actually measured based on a fractional factorial design for each of the respective semiconductor chips to which the chip numbers have been assigned;

preparing a measurement schedule and actually executing measurement to the defined measurement points;

executing an analysis of variance from obtained measurement results on the basis of the fractional factorial design; and

changing the measurement schedule on the basis of the result of the analysis of variance.

According to a seventh aspect of the present invention, there is provided a pattern inspection apparatus which is

capable to communicate with an external inspection device and which prepares a schedule to measure a pattern to supply the prepared measurement schedule to the external inspection device, said pattern inspection apparatus comprising:

a controller which receives information of a measurement point defined as a point to be actually measured to prepare a measurement schedule and supplies a first command signal to execute measurement to the defined measurement point to the external inspection device, the measurement point being defined by:

assigning first wafer numbers in order of a process with respect to a wafer group constituted of a plurality of wafers including semiconductor chip groups in which patterns are formed by a fine processing process;

dividing the wafer group into at least two first sub-groups in accordance with the first wafer numbers, and selecting at least two or more wafers having serial first wafer numbers from the first sub-group to assign second wafer numbers;

dividing the semiconductor chip group into at least two second sub-groups in accordance with distances between center positions of semiconductor chips on the wafers to which the second wafer numbers have been assigned and center positions of the wafers, selecting at least three semiconductor chips from the second sub-group, further selecting a chip including the center position of the wafer inside if any, and assigning a chip number to the selected semiconductor chip;

producing a lattice to divide a region in the selected semiconductor chip to which the chip number is assigned into rectangular regions exceeding a quantity of at least two rows and two columns based on in-chip coordinates, selecting at least four lattice points from the lattice points of the lattice, selecting a pattern in the vicinity of the selected lattice points in the pattern formed on the wafer as only one candidate measurement point with respect to the lattice

point, and assigning a candidate measurement point number to the candidate measurement point; and

selecting only some of the candidate measurement points to which the candidate measurement point numbers have been assigned based on a fractional factorial design with respect to the respective semiconductor chips to which the chip numbers have been assigned.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram showing a wafer constituting a wafer group to be measured in a first embodiment of the present invention;

FIG. 2 is a schematic diagram showing a photo mask for use in forming the wafer shown in FIG. 1;

FIG. 3 is a flowchart showing a schematic procedure of the first embodiment of the present invention;

FIGS. 4 to 6C are explanatory views of the procedure shown in the flowchart of FIG. 3;

FIGS. 7 and 8 are flowcharts showing schematic procedures of a second embodiment of the present invention;

FIG. 9 is a diagram showing one example of an orthogonal array;

FIG. 10 is a diagram showing an example of a measurement point defined based on the orthogonal array shown in FIG. 9;

FIG. 11 is a flowchart showing the schematic procedure of a fourth embodiment of the present invention; and

FIG. 12 is a block diagram showing the schematic constitution of a pattern inspection apparatus according to a sixth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Some embodiments of the present invention will hereinafter be described with reference to the drawings.

(1) First Embodiment

A first embodiment of the present invention will be

described with reference to FIGS. 1 to 7. A method of selecting a pattern to be measured with respect to a wafer group constituted of n ($n \geq 4$) wafers subjected to a lithography process will hereinafter be described. The present embodiment will be explained with an example of the wafer group constituted of n = 24 wafers.

FIG. 1 is a schematic diagram of a wafer 2 constituting the wafer group to be measured. As shown in the figure, semiconductor chips C are arranged in the wafer 2. Each chip C is formed using a photo mask 4 shown in FIG. 2. In this photo mask 4, an equivalent pattern is disposed for each of 10 rows × 10 columns sub-regions SR.

FIG. 3 is a flowchart including a schematic procedure of a method of selecting a pattern to be measured in the present embodiment.

As shown in the figure, first, wafer numbers w1, w2 ... and w24 are successively assigned to 24 wafers in order of the wafers successively processed by a lithography process (step S1).

Next, a wafer group of 24 wafers is divided into M ($M \geq 2$) sub-groups by the wafer number (step S2). In the present embodiment, the wafers are grouped in such a manner that a first group is constituted of wafers having wafer numbers w1 to w8, a second group is constituted of wafers having wafer numbers w9 to w16, and further a third group is constituted of wafers having wafer numbers w17 to w24 (M = 3).

Next, serial wafers are selected from each sub-group, and new wafer numbers are assigned (step S3). Specifically, wafers w1, w2, w3 were selected from the first sub-group to assign new wafer numbers W1, W2, W3, respectively. Similarly, wafers w12, w13 were selected from a second sub-group to assign new wafer numbers W4, W5, and further wafers w22, w23, w24 were selected from a third sub-group to assign new wafer numbers W6, W7, W8.

Next, a chip group in the wafer is divided into two (L

= 2) sub-groups in accordance with a distance from a center of the wafer (step S4). Specifically, as shown in FIG. 4, assuming that a radius of the wafer 2 is r, a boundary line BL of a virtual circular shape having a radius 1/2r in the wafer 2 and including a wafer center coordinate as an origin is defined. The chip group was divided into sub-groups CSR1 and CSR2, the sub-group CSR1 being constituted of the chips whose chip center coordinate was outside the boundary line BL, and the sub-group CSR2 being constituted of the chips whose coordinate was inside the line.

Next, k ($k \geq 3$) chips are selected from each sub-group to assign chip numbers C1 to Ck to these chips (step S5). In the present embodiment, as shown in FIG. 5, the chips were selected for every k = 4 chips, and chip numbers C1 to C8 were assigned. Furthermore, when there is the chip including the wafer center coordinate inside thereof (step S6), chip number C(k+1) is assigned to this chip (step S7). In the present embodiment, chip number 9 was assigned.

Next, the region of the chip is divided into rectangular regions the number of which exceeds 2 (rows) $\times$ 2 (columns) to form a lattice using center points of an equivalent sub-chips included in the chip (step S8). In the present embodiment, the region of the chip was divided into regions of 10 rows $\times$ 10 columns as shown in FIG. 6A.

Next, r ($r \geq 4$) lattice points are selected from lattice points obtained by dividing the lattice (step S9). In the present embodiment, as shown in FIG. 6B, eight lattice points were selected.

Next, the pattern to be measured closest to the selected lattice point is selected, and pattern numbers P1 to Pr are assigned (step S10). In the present embodiment, as shown in FIG. 6C, numbers P1 to P8 were assigned.

The quantity of candidate measurement points selected by the above-described steps S1 to S10 is $(n/M)\times(k+1)\times r$. The quantity was $8\times9\times8$ = 576 points in the present embodiment.

Next, from $(n/M)\times(k+1)\times r$ candidate measurement points,

candidate measurement point, the number of which corresponds to a divisor of $(n/M)\times(k+1)\times r$, is selected and the selected candidate measurement points is adopted as a measurement point to be actually measured (step S11). In the present embodiment, from 576 candidate measurement points, only candidate measurement points P1, P3, P5, P7 were adopted as the measurement points to be actually measured with respect to wafer numbers W1, W3, W5, W7, and only candidate measurement points P2, P4, P6, P8 were adopted as the measurement points with respect to wafer numbers W2, W4, W6, W8. As a result, the number of measurement points was 288 points.

Such design of experiment method in which only points are selected from a combination of all factors (i.e., fluctuation between the wafers: degree of freedom of 7, the fluctuation in the wafer: the degree of freedom of 8, the fluctuation in the chip: degree of freedom of 7) and the selected points are actually measured the number of which corresponds to a divisor of the combination of all the factors is called a fractional factorial design as taught by statistics. In the present embodiment, since this method is used, major effects of the factors can be checked without checking all the combinations, and therefore a measurement cost can be reduced.

Finally, the adopted 288 measurement points were actually measured (step S12).

As a result of selection of the measurement pattern by the above-described procedure, it was possible to set the total number of measurement points to 288 points although the degrees of freedom were 7, 8, 7 with respect to the dimensional fluctuations between the wafers, between the chips, and in the chip, respectively. In accordance with a conventional method, the total number is usually $(7+1)\times(8+1)\times(7+1) = 576$. Therefore, it was possible to reduce the number of measurement points to 1/2 of a conventional number.

In accordance with the present embodiment, an estimation precision of statistic in a pattern dimension or alignment deviation in one lot is thus largely enhanced.

It is to be noted that the respective steps of the flowchart shown in FIG. 3 were executed in a numerical order in the present embodiment, but the method of selecting a pattern to be measured according to the present invention does not have to be necessarily carried out in the same order as that of the procedure shown in FIG. 3.

In the present embodiment, 1/2 of all the combinations were selected for the fractional replication, but this does not limit the scope of the present invention, and the arbitrary divisor number of combinations such as 1/4, 1/8 can be selected in accordance with the cost of measurement.

Moreover, in the present embodiment, in order to enhance the estimation precision of the fluctuation of the pattern dimension and alignment deviation without increasing the cost of measurement, the numbers of wafers, chips, and patterns in the chip, which were measurement candidates, were set to 8, 9, 8, respectively. These numbers do not limit the scope of the present invention, but in order to secure the precision during calculation of the fluctuation of each factor, the respective numbers are preferably set to 8 or more. Further for a purpose of preventing the measurement cost from increasing, the numbers are preferably about 8 to 9, respectively.

For a purpose of further reducing the cost of measurement, some of the measurement points defined by the above-described method may further be selected and measured.

(2) Second Embodiment

Next, a second embodiment of the present invention will be described with reference to FIGS. 7 to 11. The present embodiment also provides the method of selecting a pattern to be measured, and characteristics thereof lie in that an orthogonal array is used to further limit and select the candidate measurement points.

FIGS. 7 and 8 are flowcharts showing schematic procedures of the method of selecting a pattern to be measured according to the present embodiment. Steps S21 to S30 shown in FIG. 7 are substantially the same as the steps S11 to S20 shown in FIG. 3, and are equivalent to steps having step numbers to each of which 10 is added. Therefore, the procedure shown in FIG. 8 will hereinafter be described.

After selecting the number corresponding to the divisor number of candidate measurement points $(n/M) \times k \times r$ candidate measurement points excluding a center chip (step S31), arbitrary three columns are selected from the orthogonal array, and a combination of these columns are used to further select the measurement points from the divisor number of the candidate measurement points excluding the center chip (step S32).

FIG. 9 shows one example of the orthogonal array. An L64 orthogonal array shown in this figure is an orthogonal array for allocating two levels and 63 factors as described in, for example, pp. 1058 to 1070 of "Design of Experiment Method, vol.2" authored by Genichi Taguchi, Maruzen Co., Ltd., 1977. It is possible to select arbitrary three columns from this L64 orthogonal array and to newly allocate the factors of eight levels by the combination of the three columns. In the present embodiment, the eight level factors newly prepared by a combination of eighth, 16th, and 23rd columns were associated with the wafer numbers W1 to W8, the eight level factors newly prepared by a combination of first, second, and fourth columns were associated with the chip numbers C1 to C8, and the eight level factors newly prepared by a combination of 27th, 32nd, and 45th columns were associated with the pattern numbers P1 to P8. As a result, 64 points were selected from 512 candidate measurement points, for example, in W1, like P1 and P4 in C1, P6 and P7 in C4, and so forth.

Furthermore, two points are selected as center shot measurement points from P1 to P8 for each wafer (step S33)

and the selected measurement points are actually measured.

By the above-described procedure, 80 measurement points were defined as shown in solid black portions of FIG. 10.

As a result, it is possible to set the number of measurement points in one lot to 80 points while the degrees of freedom are kept as 7, 8, 7 with respect to the dimensional fluctuations between the wafers, between the chips, and in the chip. Additionally, it is possible to implement the measurement without any deviation of alternate functions among the factors.

Also in the present embodiment, in order to further reduce the cost of measurement, further some points may be selected from the measurement points defined by the above-described procedure to execute the measurement.

(3) Third Embodiment

A third embodiment provides a method of preparing a schedule to measure a semiconductor pattern.

In accordance with the second embodiment, the number of the wafer to be actually measured in the wafer group, and the measurement shot in each wafer and the position in the shot were determined. Measurement point information obtained as this result is inserted, for example, into the corresponding data position in a recipe file of a CD - SEM.

This has heretofore depended on a level of skill of an engineer, and therefore there have been many errors in the prepared measurement schedule.

In accordance with the present embodiment, since the measurement schedule is prepared based on the above-described factorial design, it is possible to automatically prepare a schedule without any error. Accordingly, it is possible to easily and quickly prepare, for example, measurement recipes of a length measurement device and alignment deviation inspection device.

(4) Fourth Embodiment

The present embodiment provides an inspection method.

of a semiconductor pattern. The characteristics of the inspection method of the pattern in the present embodiment lie in that the measurement is actually executed in accordance with the measurement schedule prepared by the second embodiment, contribution ratios of fluctuation factors are judged from the measurement result, and this judgment result is used to further limit the number of measurement points.

FIG. 11 is a flowchart showing the schematic procedure of the pattern inspection method of the present embodiment.

First, the measurement schedule is prepared by the procedure shown in FIGS. 7 and 8 (step S41), and the measurement is actually executed (step S42).

Next, obtained measurement results are rearranged in order corresponding to the orthogonal array, the row of L64 orthogonal array in the present embodiment (step S43).

Next, a sum of squares corresponding to each column of the L64 orthogonal array is calculated (step S44).

Subsequently, the sum of squares, variance, standard deviation, contribution ratio are calculated corresponding to fluctuation components between the wafers, between the chips, and in the chip, and other error factors in accordance with the combination of columns of the L64 orthogonal array corresponding to the wafer number, chip number, and measurement point number (step S45), and an analysis of variance (ANOVA) table is prepared (step S46).

Next, the measurement schedule is changed based on the prepared ANOVA (step S47). For example, when the contribution ratio of the fluctuation between the wafers is turned out to be small as a result of the preparation of ANOVA, the number of wafers to be measured is changed to four from eight, 80 measurement points are changed to 40 points by the fractional factorial design, and thereafter 40 points are measured with respect to the lot processed by the same process. It is to be noted that a dummy method may be used to omit the fluctuation component between the wafers.

Finally, a graph is drawn based on magnitudes of major effects and alternate functions obtained as a result of the analysis of variance (step S48). Furthermore, after calculating average values with respect to the chip numbers C1 to C9, the average values are represented as a function of an in-wafer coordinate, and further the result of approximation of this function to a quadric surface is represented in contour. Accordingly, it is possible to more easily analyze the fluctuation components between the chips.

In accordance with the present embodiment, it is thus possible to easily analyze the fluctuation factors of the pattern dimension and alignment deviation from the actual measurement result.

(5) Fifth Embodiment

The present embodiment provides an inspection method of a semiconductor pattern, in which a measurement fluctuation is small. The characteristics of the present embodiment lie in that a dimension measurement result with respect to a calibration wafer constituting a standard for a measured value is used to judge precision of measurement in accordance with the measurement schedule obtained by the second embodiment prior to actual measurement.

First, the calibration wafer constituting the standard for the measured value is used to repeatedly measure the dimension of the same portion 20 times, and a ratio of a value obtained by multiplying a standard deviation σ by 5.15 to a dimensional tolerance is obtained.

Next, a dimensional precision of measurement by the above-described measurement schedule is estimated from the ratio of obtained 5.15 σ to the dimensional tolerance. For example, when the ratio of 5.15 σ to the dimensional tolerance is 42%, it is found that there is no precision in the dimension obtained by the measurement in accordance with the measurement schedule prepared in the second embodiment.

To solve the problem, the measurement is repeated twice in accordance with to the measurement schedule

prepared based on the L64 orthogonal array, and the average value of two measurements is adopted as the measurement value. Accordingly, the same effect as that in substantially reducing the measurement fluctuation to 30% from 42% is obtained, and the cost of measurement can be reduced.

(6) Sixth Embodiment

A sixth embodiment provides a pattern inspection apparatus which implements the method of selecting a pattern to be measured and the pattern inspection method.

FIG. 12 is a block diagram showing the schematic constitution of the pattern inspection apparatus of the present embodiment. A pattern inspection apparatus 10 shown in the figure comprises a computer 16, recording equipment 18 such as a hard disk drive connected to the computer 16, a terminal device 12 connected to the computer 16, and a display unit 14 connected to the terminal device 12.

The recording equipment 18 stores recipe files of a measurement schedule preparation program, ANOVA program, table/graph preparation program and a data table of the orthogonal array.

The computer 16 receives the measurement point information, reads the measurement schedule preparation program from the recording equipment 18 and prepares the measurement schedule by selecting the pattern to be measured with reference to the data table of the orthogonal array.

The computer 16 is connected to an external measurement device 100, and supplies the prepared measurement schedule as measurement recipe data to the measurement device 100. The measurement device 100 inserts the measurement recipe data into the corresponding data position of the recipe file (not shown), actually executes the measurement to the wafer group, and feeds back the measurement result to the computer 16. The computer 16 extracts the ANOVA program and table/graph preparation program from the recording equipment 18, and executes the ANOVA described in the fourth embodiment based on the

measurement result sent from the measurement device 100 to prepare a table and graph on the basis of the obtained ANOVA. The ANOVA result and the table/graph are supplied to the terminal device 12 and displayed by the display unit 14.

The computer 16 can also change the measurement schedule in accordance with the procedure by the above-described fourth embodiment. In this case, the changed measurement schedule is supplied as new measurement recipe data to the measurement device 100.

The computer 16 can also judge the dimensional precision of the measurement implemented by the prepared measurement schedule in accordance with the fifth embodiment prior to the actual measurement. In this case, when the estimated dimensional precision is low, the measurement device 100 executes the measurement twice in accordance with the measurement schedule based on the orthogonal array, and the computer 16 calculates the average value of the sent results of two measurements, and displays this value as the measurement value in the display unit 14 via the terminal device 12.

In accordance with the present embodiment, the cost of measurement is thus reduced, and the fluctuation factor can easily be diagnosed. Therefore, it is possible to execute pattern inspection with high estimation precision of statistic by a simple arrangement, for example, in the pattern dimension and alignment deviation with respect to the wafers in one lot.

(7) Program and Recording Medium

A series of procedure of the method of selecting a pattern to be measured or the pattern inspection method may also be incorporated in the program and read and executed by a computer. Accordingly, the method of selecting a pattern to be measured or the pattern inspection method according to the present invention can be realized using a general-purpose computer. Moreover, the series of procedure of the method of selecting a pattern to be measured or the pattern

inspection method may also be stored as a program to be executed by a computer in a recording medium such as a flexible disk and CD-ROM, and read and executed by the computer.

The recording media are not limited to portable media such as a magnetic disk and optical disk, and may also be fixed recording media such as a hard disk drive and memory. The program in which the series of procedure of the method of selecting a pattern to be measured or the pattern inspection method is incorporated may also be distributed via communication circuits such as internet (including radio communication). Furthermore, the program in which series of procedure of the method of selecting a pattern to be measured or the pattern inspection method is incorporated may be encrypted, modified, or compressed. In this state, the program may also be stored in the recording media and distributed via wires such as internet or via radio.

(8) Method of Manufacturing Semiconductor Device

When a semiconductor device is manufactured by a process including a low-cost/high-precision inspection process using the method of selecting a pattern to be measured or the pattern inspection method, the semiconductor device can be manufactured with high throughput and yield.

Several embodiments of the present invention have been described above, but the present invention is not limited to the above-described modes, and can, needless to say, be modified and carried out variously without departing from the scope thereof. In the above embodiment, a CD-SEM and an alignment deviation inspection apparatus are exemplified as specific examples of the inspection apparatus, but the present invention can also be applied, for example, to an optical apparatus called scatterometry.